NEC

MOS INTEGRATED CIRCUIT

μPD16520,16520A

VERTICAL DRIVER FOR CCD SENSORS

DESCRIPTION

The μPD16520 and μPD16520A are vertical drivers for CCD image sensors that have a level conversion circuit and a 3-level output function. Since it incorporates a CCD vertical register driver equivalent to the μPD16510 (10 channels, consisting of six 3-level channels and four 2-level channels) and a VOD shutter driver (1 channel), it is ideal as a vertical driver for multiple-electrode high-pixel CCD transfer type area image sensors employed in digital still cameras.

The μPD16520 and μPD16520A use a CMOS process to achieve optimum transmission delay characteristics for vertical driving of CCD image sensors, as well as output on-state resistance characteristics. The μPD16520 and μPD16520A also support low-voltage logic (logic power supply voltage: 2.0 to 5.5 V).

FEATURES

- CCD vertical register driver: 10 channels (3-level: 6 channels, 2-level: 4 channels)
- VOD shutter driver: 1 channel
- High withstanding voltage: 33 V MAX.
- Low-output on-state resistance: 30 Ω TYP.
- Low-voltage input supported (Logic power supply voltage: 2.0 to 5.5 V)
- Latch-up free
- Same drive capacity as μPD16510
- Small package: 38-pin plastic SSOP (7.62 mm (300))
- Super small package: 42-pin wafer level CSP

APPLICATIONS

Digital still cameras, digital video cameras, etc.

ORDERING INFORMATION

Part Number	Package
μPD16520GS-BGG	38-pin plastic SSOP (7.62 mm (300))
μPD16520AFH-2Q1	42-pin wafer level CSP

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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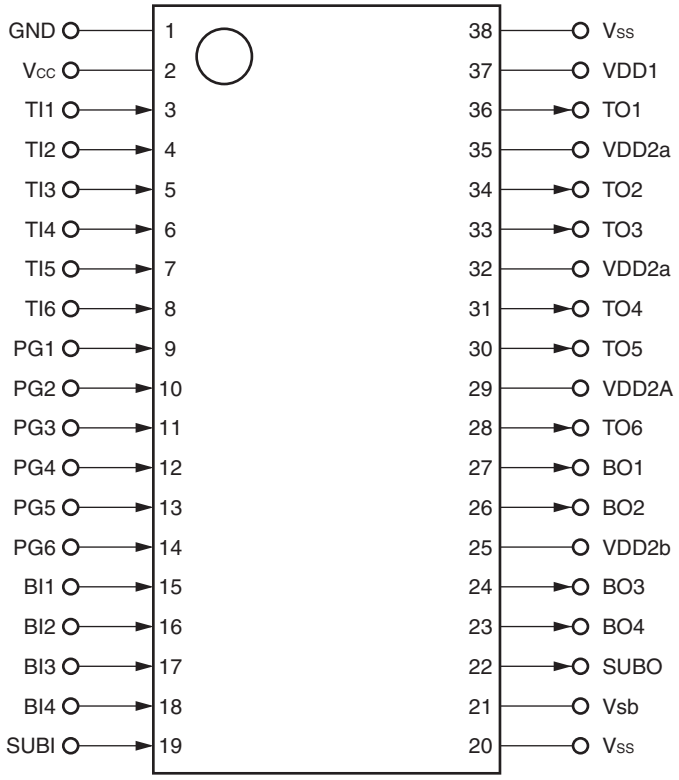
Printed in Japan

The mark ★ shows major revised points.

1. PIN CONFIGURATION

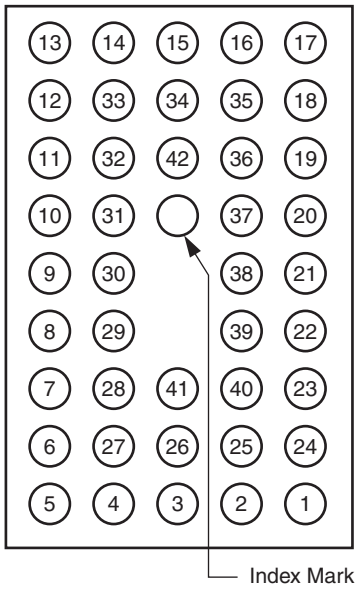
(1) 38-pin plastic SSOP (7.62 mm (300))

μPD16520GS-BGG (Top view)



(2) 42-pin wafer level CSP

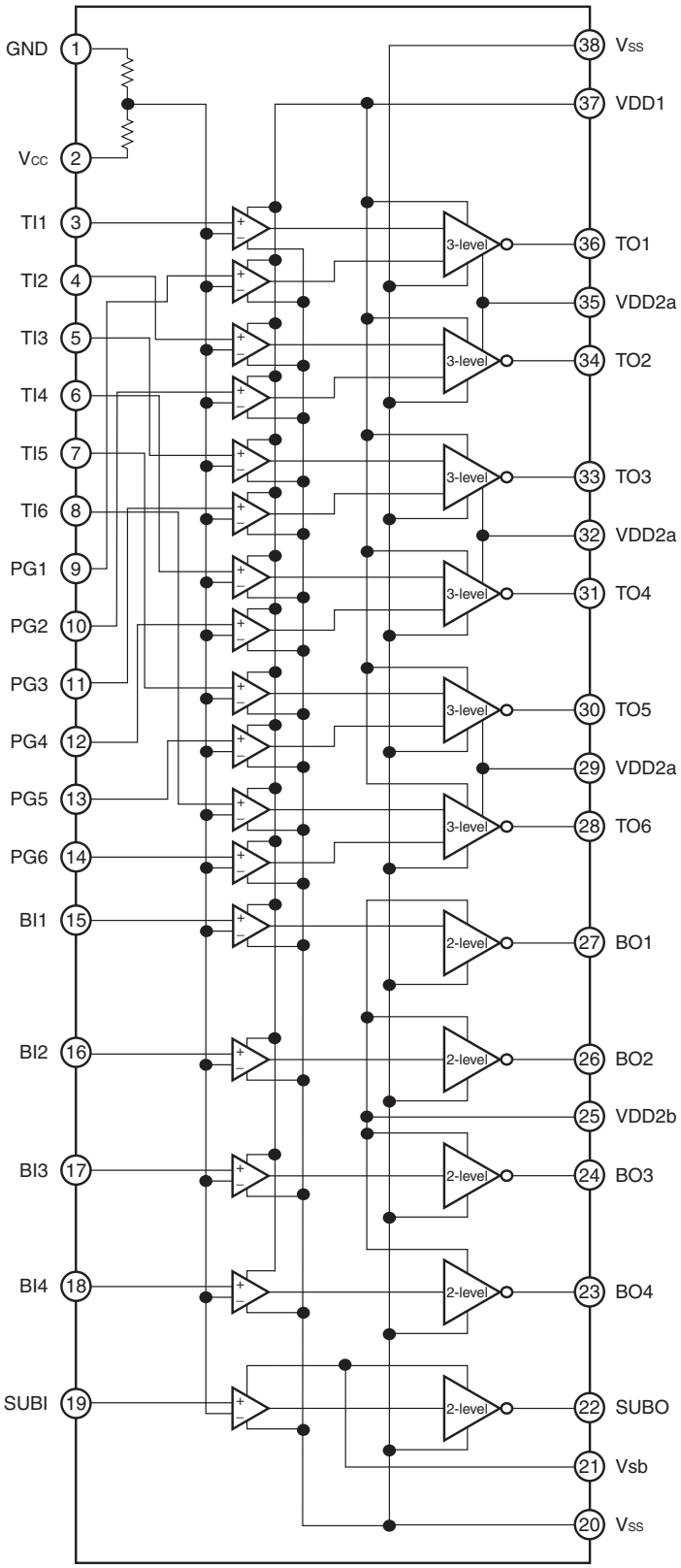
μPD16520AFH-2Q1 (Bottom view)



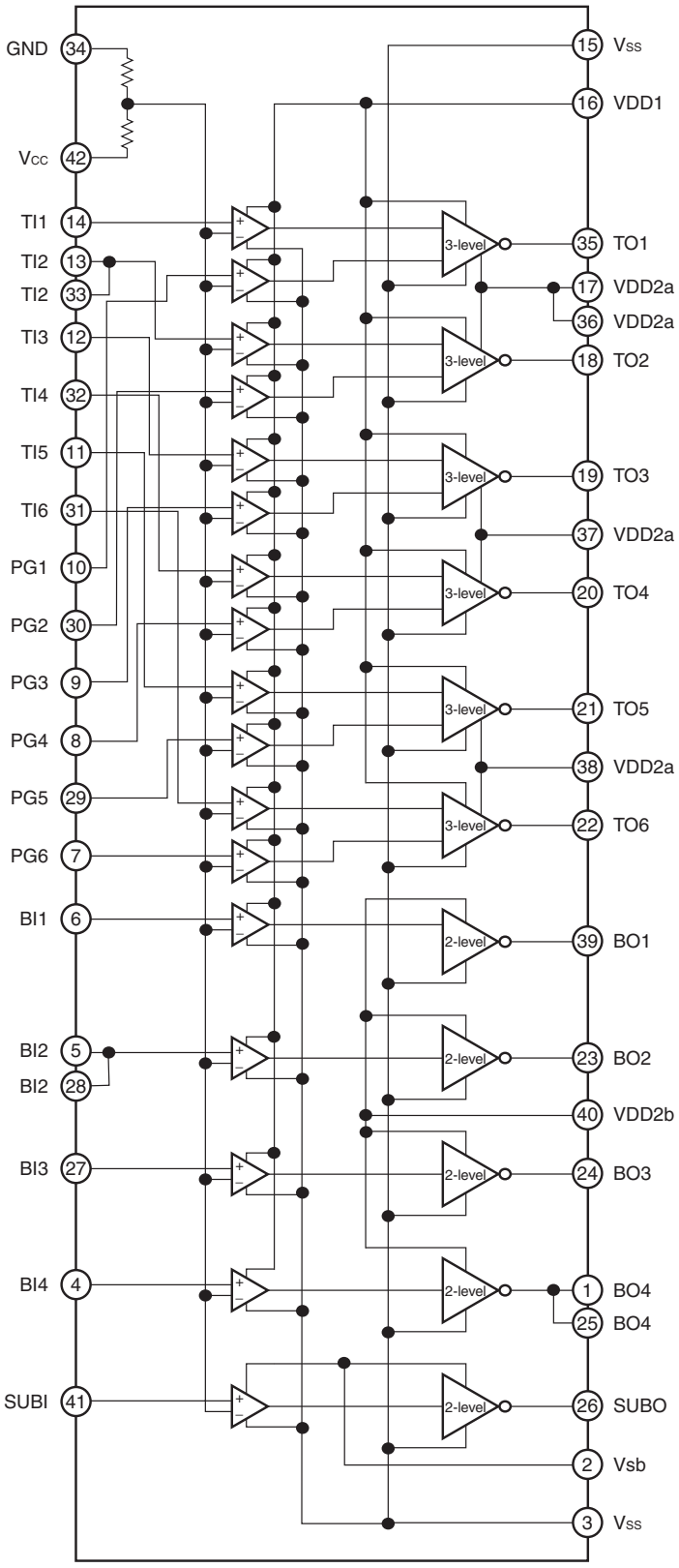
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	BO4	15	V_{SS}	29	PG5
2	Vsb	16	VDD1	30	PG2
3	V_{SS}	17	VDD2a	31	TI6
4	BI4	18	TO2	32	TI4
5	BI2	19	TO3	33	TI2
6	BI1	20	TO4	34	GND
7	PG6	21	TO5	35	TO1
8	PG4	22	TO6	36	VDD2a
9	PG3	23	BO2	37	VDD2a
10	PG1	24	BO3	38	VDD2a
11	TI5	25	BO4	39	BO1
12	TI3	26	SUBO	40	VDD2b
13	TI2	27	BI3	41	SUBI
14	TI1	28	BI2	42	V_{CC}

2. BLOCK DIAGRAM

(1) μPD16520GS-BGG



(2) μPD16520AFH-2Q1



3. PIN FUNCTIONS

(1) μPD16520GS-BGG

Pin No.	Pin Name	I/O	Function
1	GND	–	Ground
2	V_{CC}	–	Logic power supply
3	TI1	Input	3-level driver input (for charge transfer) (Refer to **4. FUNCTION TABLES**.)
4	TI2	Input	
5	TI3	Input	
6	TI4	Input	
7	TI5	Input	
8	TI6	Input	
9	PG1	Input	3-level driver input (for charge read) (Refer to **4. FUNCTION TABLES**.)
10	PG2	Input	
11	PG3	Input	
12	PG4	Input	
13	PG5	Input	
14	PG6	Input	
15	BI1	Input	2-level driver input (for charge transfer) (Refer to **4. FUNCTION TABLES**.)
16	BI2	Input	
17	BI3	Input	
18	BI4	Input	
19	SUBI	Input	VOD shutter drive pulse input
20	V_{SS}	–	V_L power supply
21	Vsb	–	V_{HH} power supply (for SUB drive)
22	SUBO	Output	VOD shutter drive pulse output
23	BO4	Output	2-level pulse output
24	BO3	Output	
25	VDD2b	–	V_{Mb} power supply (for 2-level driver)
26	BO2	Output	2-level pulse output
27	BO1	Output	
28	TO6	Output	3-level pulse output
29	VDD2a	–	V_{Ma} power supply (for 3-level driver)
30	TO5	Output	3-level pulse output
31	TO4	Output	
32	VDD2a	–	V_{Ma} power supply (for 3-level driver)
33	TO3	Output	3-level pulse output
34	TO2	Output	
35	VDD2a	–	V_{Ma} power supply (for 3-level driver)
36	TO1	Output	3-level pulse output
37	VDD1	–	V_H power supply
38	V_{SS}	–	V_L power supply

(2) μPD16520AFH-2Q1

Pin No.	Pin Name	I/O	Function
1	BO4	Output	2-level pulse output
2	Vsb	–	V_{HH} power supply (for SUB drive)
3	V_{SS}	–	V_L power supply
4	BI4	Input	2-level driver input (for charge transfer)
5	BI2	Input	(Refer to **4. FUNCTION TABLES**.)
6	BI1	Input	
7	PG6	Input	3-level driver input (for charge read)
8	PG4	Input	(Refer to **4. FUNCTION TABLES**.)
9	PG3	Input	
10	PG1	Input	
11	TI5	Input	3-level driver input (for charge transfer)
12	TI3	Input	(Refer to **4. FUNCTION TABLES**.)
13	TI2	Input	
14	TI1	Input	
15	V_{SS}	–	V_L power supply
16	VDD1	–	V_H power supply
17	VDD2a	–	V_{Ma} power supply (for 3-level driver)
18	TO2	Output	3-level pulse output
19	TO3	Output	
20	TO4	Output	
21	TO5	Output	
22	TO6	Output	
23	BO2	Output	2-level pulse output
24	BO3	Output	
25	BO4	Output	
26	SUBO	Output	VOD shutter drive pulse output
27	BI3	Input	2-level driver input (for charge transfer)
28	BI2	Input	(Refer to **4. FUNCTION TABLES**.)
29	PG5	Input	3-level driver input (for charge read)
30	PG2	Input	(Refer to **4. FUNCTION TABLES**.)
31	TI6	Input	3-level driver input (for charge transfer)
32	TI4	Input	(Refer to **4. FUNCTION TABLES**.)
33	TI2	Input	
34	GND	–	Ground
35	TO1	Output	3-level pulse output
36	VDD2a	–	V_{Ma} power supply (for 3-level driver)
37	VDD2a	–	
38	VDD2a	–	
39	BO1	Output	2-level pulse output
40	VDD2b	–	V_{Mb} power supply (for 2-level driver)
41	SUBI	Input	VOD shutter drive pulse input
42	V_{CC}	–	Logic power supply

4. FUNCTION TABLE ($V_L = V_{SS}$, $V_{Ma} = V_{DD2a}$, $V_{Mb} = V_{DD2b}$, $V_H = V_{DD1}$, $V_{HH} = V_{sb}$)

Pins TO1 to TO6

	Input												Output					
Pin Name	TI1	TI2	TI3	TI4	TI5	TI6	PG1	PG2	PG3	PG4	PG5	PG6	TO1	TO2	TO3	TO4	TO5	TO6
Pin No.	3	4	5	6	7	8	9	10	11	12	13	14	36	34	33	31	30	28
	14	13, 33	12	32	11	31	10	30	9	8	29	7	35	18	19	20	21	22
	L						L						V_H					
	L						H						V_{Ma}					
	H						L						V_L					
	H						H											

Remark Pin No. upper row: μPD16520GS-BGG, lower row: μPD16520AFH-2Q1

Pins BO1 to BO4

	Input				Output			
Pin Name	BI1	BI2	BI3	BI4	BO1	BO2	BO3	BO4
Pin No.	15	16	17	28	27	26	24	23
	6	5, 28	27	4	39	23	24	1, 25
	L				V_{Ma}			
	H				V_L			

Remark Pin No. upper row: μPD16520GS-BGG, lower row: μPD16520AFH-2Q1

Pin SUBO

	Input	Output
Pin Name	SUBI	SUBO
Pin No.	19	22
	41	26
	L	V_{HH}
	H	V_L

Remark Pin No. upper row: μPD16520GS-BGG, lower row: μPD16520AFH-2Q1

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{SS}		0 to −10	V
	V_{CC}		V_{SS} − 0.3 to V_{SS} + 20.0	V
	VDD1		V_{SS} − 0.3 to V_{SS} + 33.0	V
	VDD2		V_{SS} − 0.3 to V_{SS} + 33.0	V
	Vsb		V_{SS} − 0.3 to V_{SS} + 33.0	V
Input pin voltage	V_I		V_{SS} − 0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		−25 to +85	°C
Storage temperature	T_{stg}		−40 to +125	°C
Allowable dissipation	P_d	μPD16520GS-BGG	500	mW
		μPD16520AFH-2Q1	600 Note	mW

Note Mounted on 8-layer glass epoxy board of 30 mm x 30 mm x 1.6 mm

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = 25°C, GND = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}		2.0		5.5	V
	VDD1	**Note**	10.5	15.0	21.0	V
	VDD1-V_{SS}	**Note**	16.5		31.0	V
	VDD2a		−1.0		+4.0	V
	VDD2b		−1.0		+4.0	V
	V_{SS}		−10.0		−6.0	V
	Vsb-V_{SS}	**Note**			31.0	V
High level input voltage	V_{IH}		0.8 V_{CC}		V_{CC}	V
Low level input voltage	V_{IL}		0		0.3 V_{CC}	V
Operating ambient temperature	T_A		−20		+70	°C

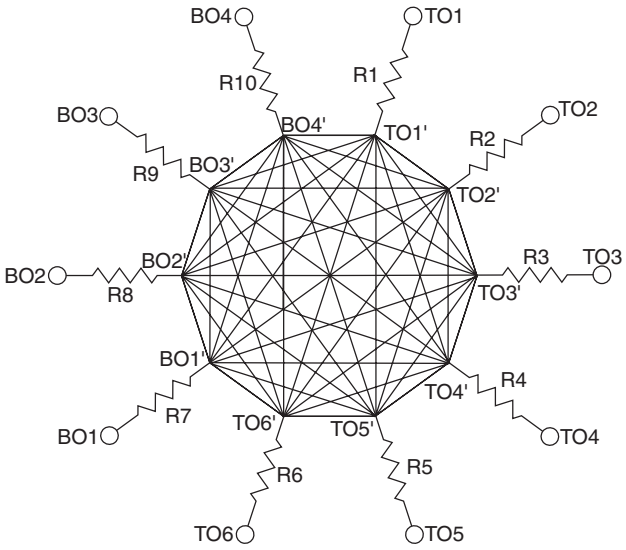
Note Set VDD1 and V_{SS} to values that satisfy VDD1-V_{SS} rating.

Electrical Characteristics (Unless otherwise specified, T_A = 25°C, VDD1 = +15 V, VDD2a = 0 V, VDD2b = +1.0 V, Vsb = 21.5 V, V_{CC} = +2.5 V, V_{SS} = –7.0 V, GND = 0 V)

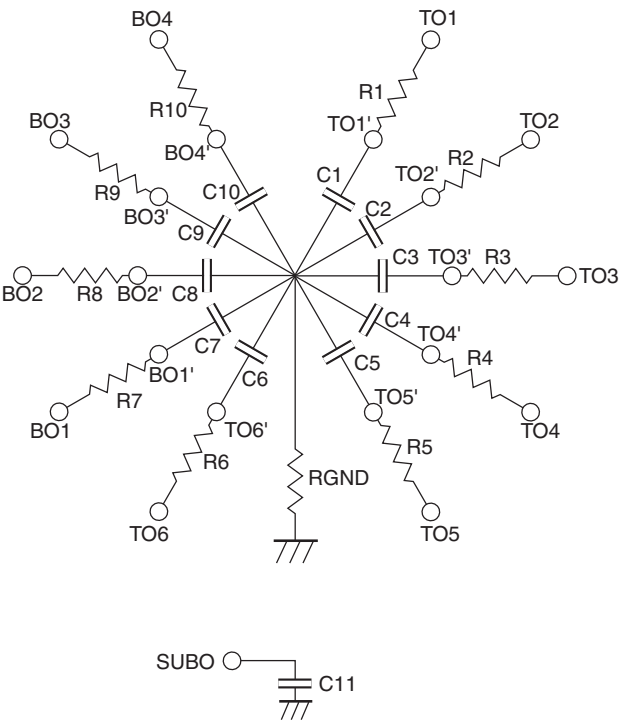
	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	High level output voltage	V_H	I_O = –20 μA	VDD1 – 0.1		VDD1	V
	Middle level output voltage	V_{Ma}	I_O = –20 μA	VDD2a – 0.1		VDD2a	V
		V_{Mb}	I_O = 20 μA	VDD2b		VDD2b + 0.1	V
	Low level output voltage	V_L	I_O = 20 μA	V_{SS}		V_{SS} + 0.1	V
	SUB high level output voltage	V_{subH}	I_O = –20 μA	Vsb – 0.1		Vsb	V
	SUB low level output voltage	V_{subL}	I_O = 20 μA	V_{SS}		V_{SS} + 0.1	V
★	Output on-state resistance	R_L	I_O = 10 mA		20	30	Ω
		R_M	I_O = ±10 mA		30	45	Ω
		R_H	I_O = –10 mA		30	40	Ω
		R_{sub}			30	40	Ω
	Transmission delay time 1	TD1	No load,			200	ns
	Transmission delay time 2	TD2	Refer to **Figure 5–2. Timing Chart**.			200	ns
	Transmission delay time 3	TD3				200	ns
	Rise/fall time 1	TP1	Refer to **Figure 5–1. Output Load**			500	ns
	Rise/fall time 2	TP2	**Equivalence Circuit** and			500	ns
	Rise/fall time 3	TP3	**Figure 5–2. Timing Chart**.			200	ns

Figure 5–1. Output Load Equivalence Circuit

(a) Between output pins



(b) Between output pin and GND



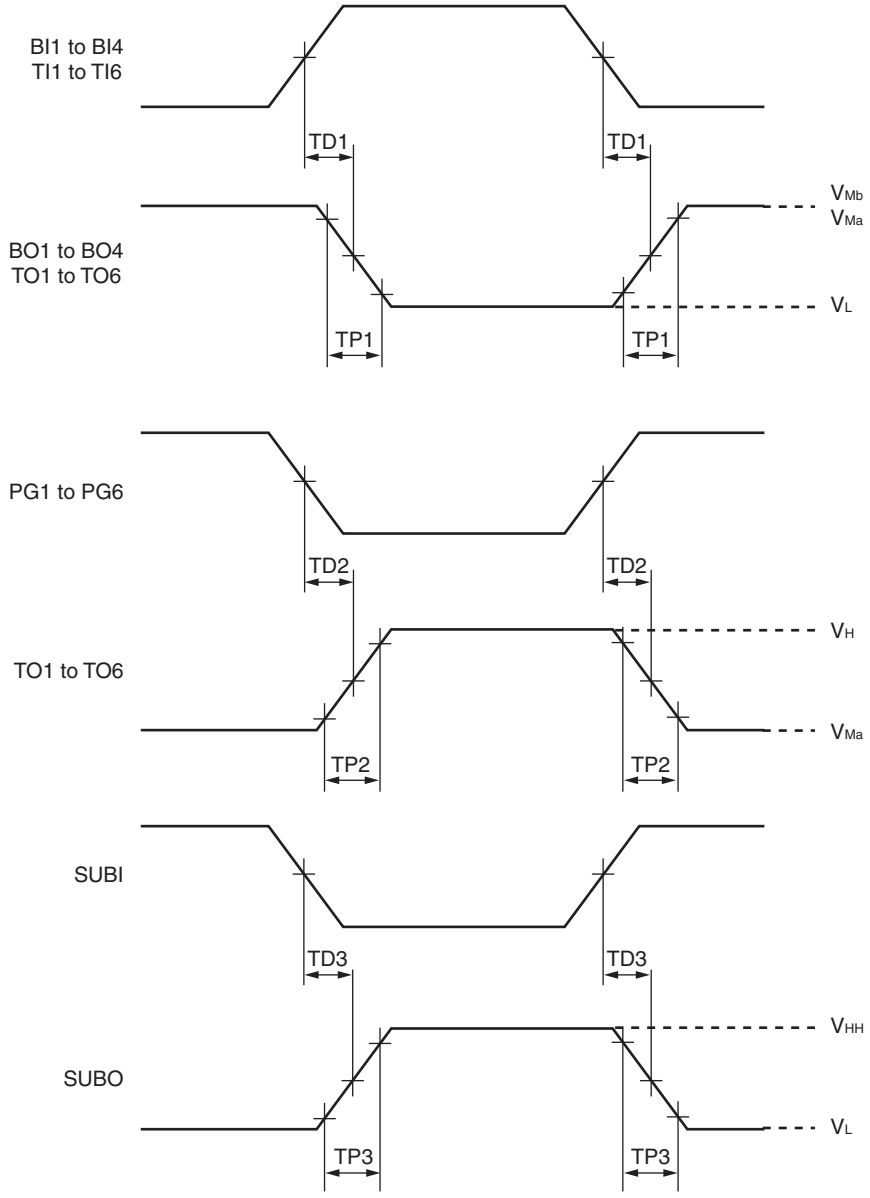
Output Load Capacitance Symbol

	TO1'	TO2'	TO3'	TO4'	TO5'	TO6'	BO1'	BO2'	BO3'	BO4'	GND
TO1'	–	C_33	C_33	C_33	C_33	C_33	C_32	C_23	C_32	C_23	C1
TO2'	C_33	–	C_33	C_33	C_33	C_33	C_23	C_32	C_23	C_32	C2
TO3'	C_33	C_33	–	C_33	C_33	C_33	C_32	C_23	C_32	C_23	C3
TO4'	C_33	C_33	C_33	–	C_33	C_33	C_23	C_32	C_23	C_32	C4
TO5'	C_33	C_33	C_33	C_33	–	C_33	C_32	C_23	C_32	C_23	C5
TO6'	C_33	C_33	C_33	C_33	C_33	–	C_23	C_32	C_23	C_32	C6
BO1'	C_32	C_23	C_32	C_23	C_32	C_23	–	C_22	C_22	C_22	C7
BO2'	C_23	C_32	C_23	C_32	C_23	C_32	C_22	–	C_22	C_22	C8
BO3'	C_32	C_23	C_32	C_23	C_32	C_23	C_22	C_22	–	C_22	C9
BO4'	C_23	C_32	C_23	C_32	C_23	C_32	C_22	C_22	C_22	–	C10
SUBO	–	–	–	–	–	–	–	–	–	–	C11

Output Load Equivalence Circuit Constants

Parameter	Symbol	Constant
Vertical register serial resistor	R1 to R10	0 Ω
Vertical register ground resistor	PGND	0 Ω
Capacitance 1 between vertical register clocks (3-level - 3-level)	C_33	0 pF
Capacitance 2 between vertical register clocks (2-level - 2-level)	C_22	0 pF
Capacitance 3 between vertical register clocks (3-level - 2-level)	C_32	1000 pF
Capacitance 4 between vertical register clocks (2-level - 3-level)	C_23	500 pF
Vertical register ground capacitance 1 (3-level)	C1 to C6	3000 pF
Vertical register ground capacitance 2 (2-level)	C7 to C10	1500 pF
Substrate ground capacitance	C11	1600 pF

Figure 5–2. Timing Chart



6. NOTE ON USE

6.1 Power ON/OFF Sequence

In the μPD16520 and μPD16520A, a PN junction (diode) exists between VDD2 → VDD1, input pin (TI1 to TI6, PG1 to PG6, BI1 to BI4, and SUBI) → VCC, so that in the case of voltage conditions: VDD2 > VDD1, input pin voltage (TI1 to TI6, PG1 to PG6, BI1 to BI4, and SUBI) > VCC, an abnormal current flows. Therefore, when turning the power ON/OFF, make sure that the following voltage conditions are satisfied: VDD2 ≤ VDD1, input pin voltage (TI1 to TI6, PG1 to PG6, BI1 to BI4, and SUBI) ≤ VCC. Also, to minimize the negative potential applied to the SUB pin of the CCD image sensor, following the power ON/OFF sequence described below.

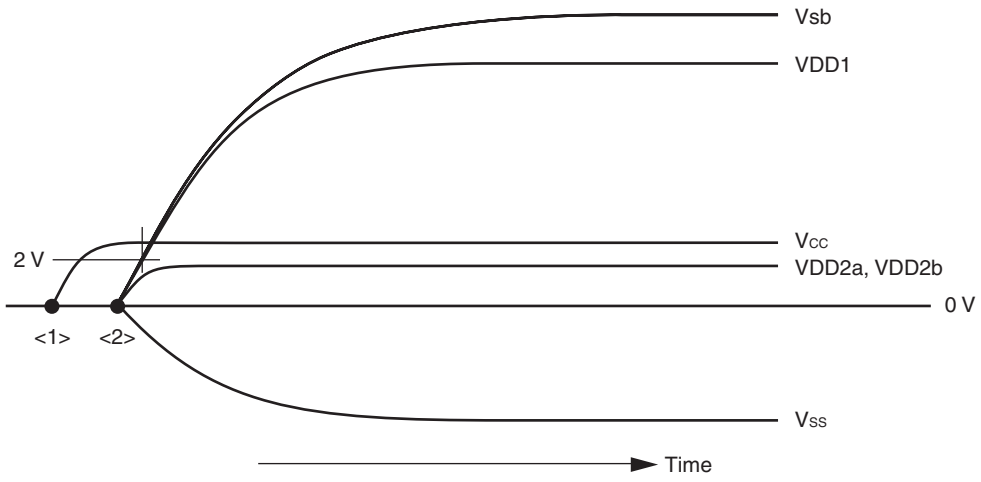
(1) Power ON

<1> Powering ON VCC

Make sure that input pin voltage (TI1 to TI6, PG1 to PG6, BI1 to BI4, and SUBI) ≤ VCC. Also, when Vsb = 2 V, make sure that VCC reaches the rated voltage.

<2> Powering ON Vsb, VDD1, VDD2a, VDD2b and VSS

At this time, make SUBI high level (0.8VCC or higher) .



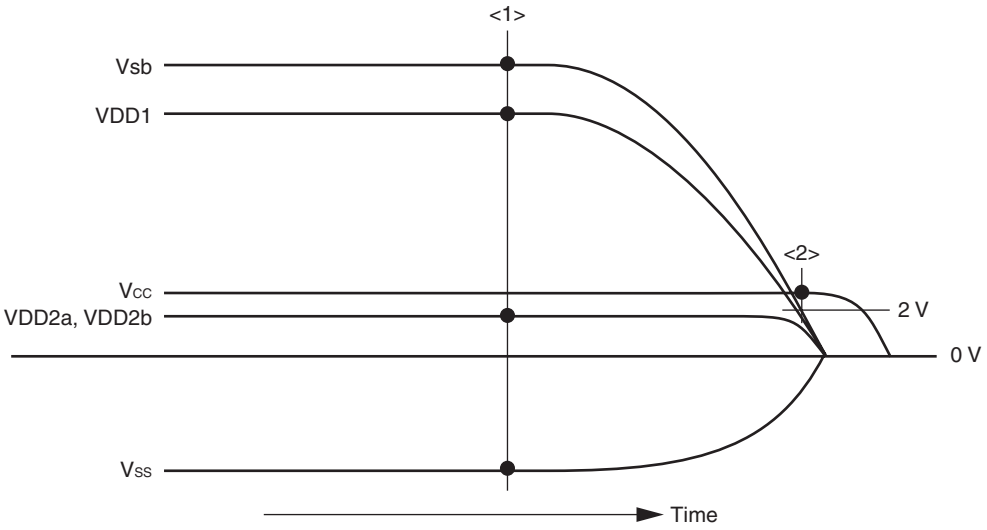
(2) Power OFF

<1> Powering OFF Vsb, VDD1, VDD2a, VDD2b and Vss

Until Vcc power OFF, keep SUBI high level (0.8Vcc or higher) .

<2> Powering OFF Vcc

Power OFF Vcc when Vsb becomes 2 V or lower. At this time, make sure that the input pin voltage (TI1 to TI6, PG1 to PG6, BI1 to BI4, and SUBI) ≤ Vcc.



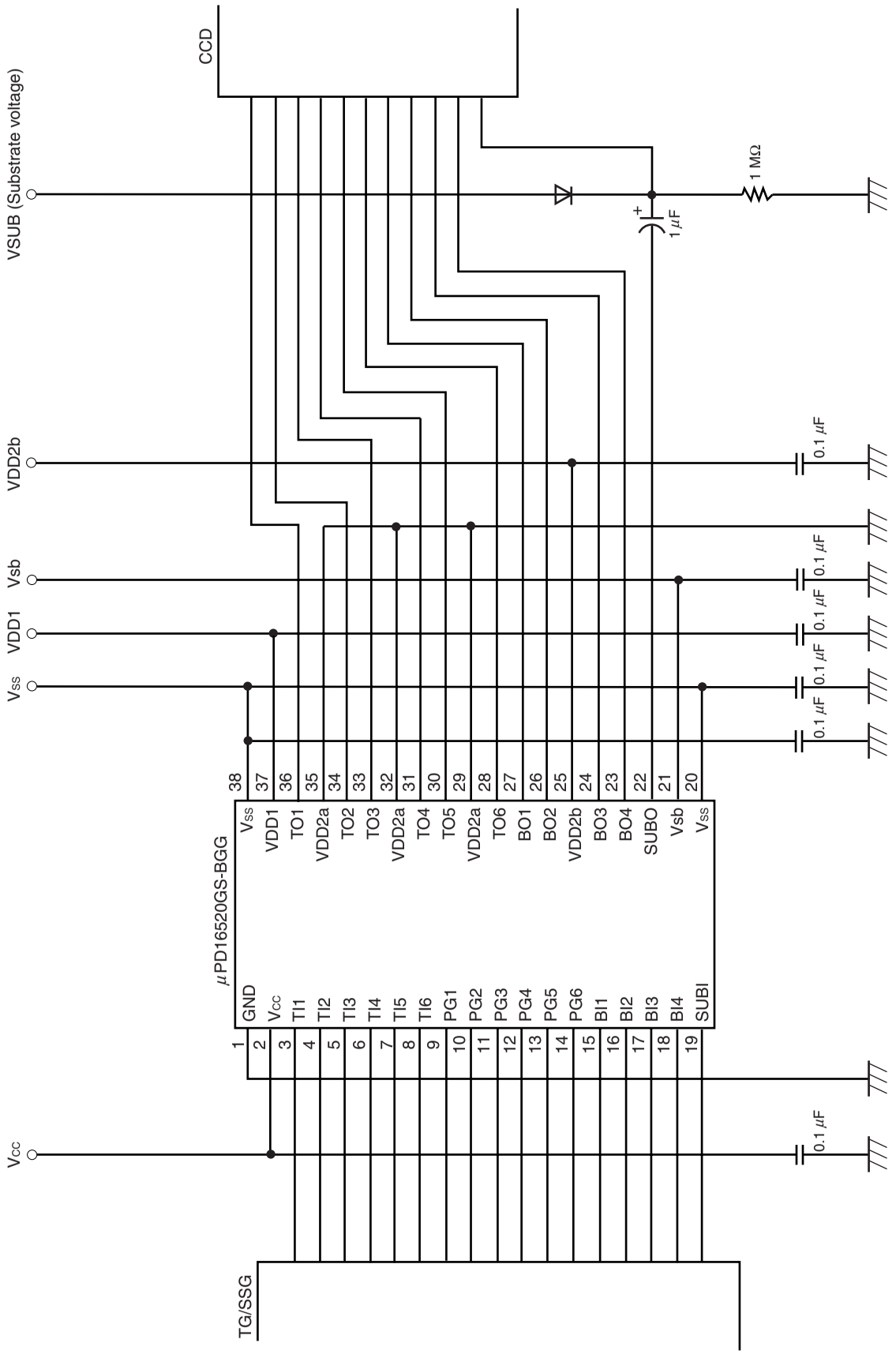
6.2 Recommended Connection of Unused Pins

Handle input pins and output pins that are not used as follows.

Input pin: High level (connect to Vcc)

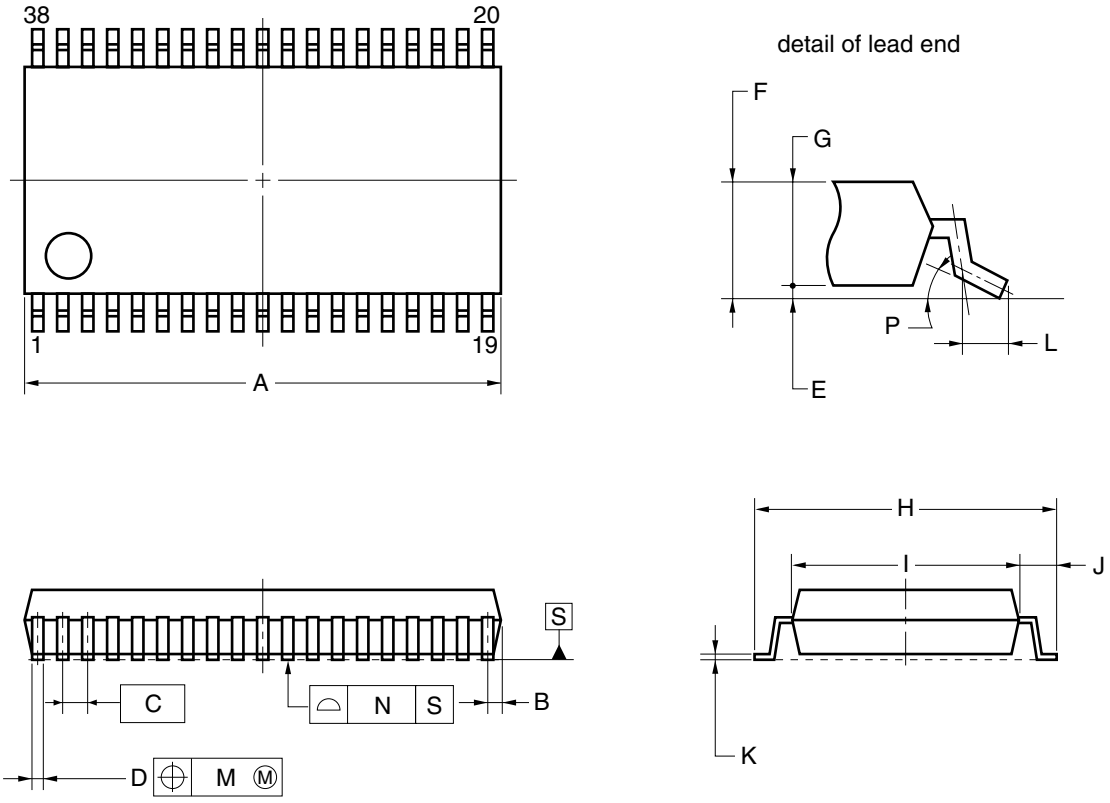
Output pin: Leave open

7. APPLICATION CIRCUIT EXAMPLE



8. PACKAGE DRAWINGS

38-PIN PLASTIC SSOP (7.62 mm (300))



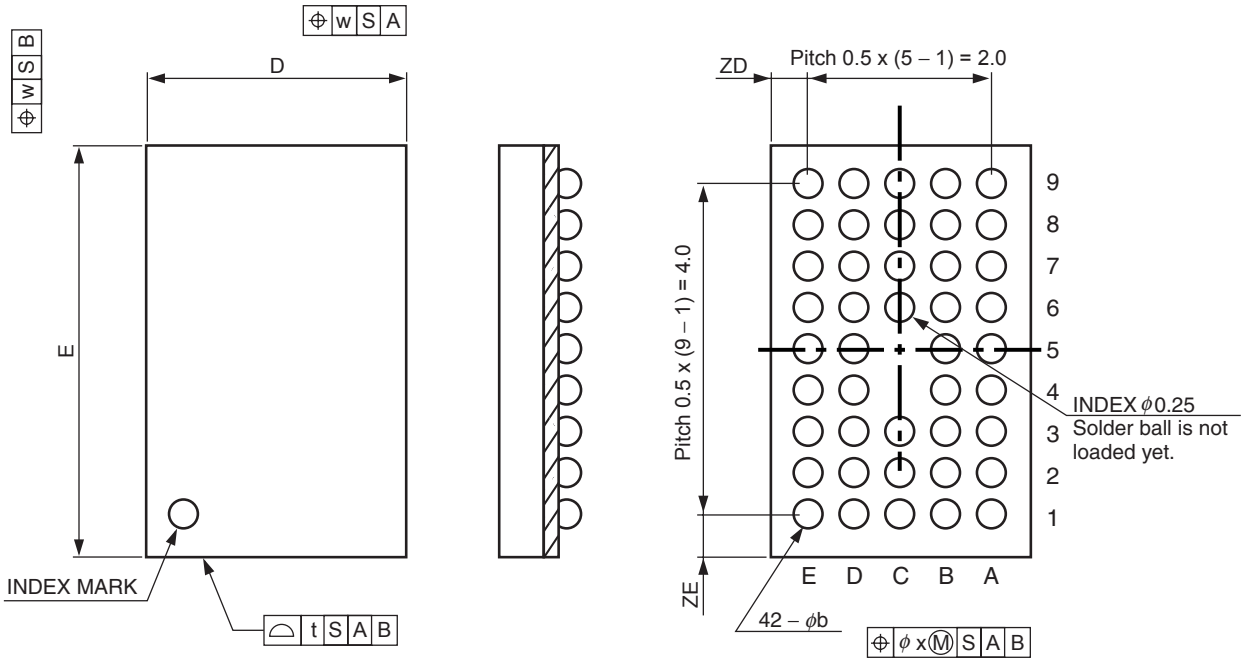
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

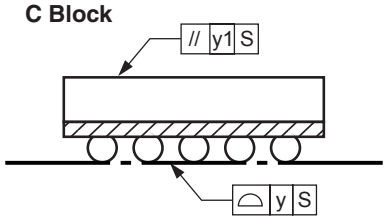
ITEM	MILLIMETERS
A	12.7±0.3
B	0.65 MAX.
C	0.65 (T.P.)
D	$0.37^{+0.05}_{-0.1}$
E	0.125±0.075
F	1.675±0.125
G	1.55
H	7.7±0.2
I	5.6±0.2
J	1.05±0.2
K	$0.2^{+0.1}_{-0.05}$
L	0.6±0.2
M	0.10
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P38GS-65-BGG-1

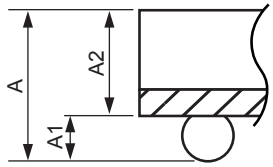
42-PIN WAFER LEVEL CSP (Unit: mm)



C Block



C Block Details



	Standard		
Parameter	MIN.	TYP.	MAX.
D	2.98	3.03	3.08
E	4.99	5.04	5.09
ZD	–	0.515	–
ZE	–	0.520	–
e		0.5	
t			0.15
A	0.66	0.73	0.8
A1	0.18	0.23	0.28
A2	0.48	0.50	0.52
b	0.25	0.30	0.35
y	–	–	0.08
x	–	–	0.05
w	–	–	0.20
y1	–	–	0.20

9. RECOMMENDED SOLDERING CONDITIONS

The μPD16520 and μPD16520A should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD16520GS-BGG: 38-pin plastic SSOP (7.62 mm (300))

Process	Conditions	Symbol
Infrared reflow	Peak temperature: 235°C or below (package surface temperature) , Reflow time: 30 seconds or less (at 210°C or higher) , Maximum number of reflow processes: 3 times or less.	IR35-00-3
Vapor phase soldering	Peak temperature: 215°C or below (package surface temperature) , Reflow time: 40 seconds or less (at 200°C or higher) , Maximum number of reflow processes: 3 times or less.	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120° or below (package surface temperature) .	WS60-00-1
Partial heating method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each side of the device) .	–

μPD16520AFH-2Q1: 42-pin wafer level CSP

Process	Conditions	Symbol
Infrared reflow	Peak temperature: 260°C or below (package surface temperature) , Reflow time: 60 seconds or less (at 220°C or higher) , Maximum number of reflow processes: 3 times or less.	IR60-00-3

Caution Do not use different soldering methods together (except for partial heating) .

REFERENCE DOCUMENTS

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades on NEC Semiconductor Devices (C11531E)

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.